REMARKS

The Examiner objects to the specification under 37 CFR § 1.71.

The Examiner objects to the drawings under 37 CFR § 1.83.

Claims 1-35 are pending in the application.

The Examiner objects to claims 10, 18, 28 and 31 for a variety of informalities.

The Examiner rejects claims 3-20 and 23-35 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner rejects claims 1, 5, 9, 23, 24 and 28-35 under 35 U.S.C. §102(e) as being anticipated by Date (U.S. Patent No. 6,438,635).

The Examiner rejects claims 2 and 10-12 under 35 U.S.C. §103(a) as being unpatentable over Date in view of Novak (U.S. Patent No. 6,046,952).

The Examiner rejects claims 3, 4, and 25-27 under 35 U.S.C. §103(a) as being unpatentable over Date in view of Kelley (U.S. Patent No. 6,081,863).

The Examiner rejects claims 6-8 and 13-17 under 35 U.S.C. §103(a) as being unpatentable over Date in view of Morita (U.S. Patent No. 6,003,116).

The Examiner rejects claims 18-22 under 35 U.S.C. §103(a) as being unpatentable over Date in view of Neal (U.S. Patent No. 6,195,723).

Applicants amend claims 3, 4, 5, 10, 12, 18, 23, 24, 26, 27, 28, 31 and 34. Claims 1-35 remain in the case

Applicants add no new matter and request reconsideration.

Specification and Drawing Objections

Applicants amend the specification and drawings to obviate the Examiner's objections as described in paragraphs 1-6 of the office action.

Claim Objections

Applicants amend the claims to obviate the Examiner's objections.

Claim Rejections Under § 112

Applicants amend the claims to obviate the Examiner's rejections under §112.

Claim Rejections Under § 102 and 103(a)

Claim 1 recites *a system bus on the chip coupled with the first blocks* and *an external bus for coupling a dual one of the first blocks to a plurality of second blocks external to the chip.* Claims 5 and 34 recite similar limitations. The Examiner alleges Date's G Bus 404 discloses the recited system bus. According to the Examiner, the first blocks are akin to Date's system bus bridge 402 and bus masters 1-4. Date, Fig. 35. The Examiner further contends that the IO Bus 405 discloses the recited external bus for coupling one of the first blocks, i.e., a system bus bridge 402, to a plurality of the second blocks external to the chip. Date, Fig. 35. The IO Bus 405, however, does not couple to any blocks *external to the chip* and therefore cannot disclose the external bus recited in claim 1. Date, Fig. 4, item 405.

Date's bus labeled "Memory Bus" appears more like the external bus recited. But Date's Memory Bus is coupled between the memory controller 403 and the system memory 3501. Date, Fig. 4 and Fig. 35. The memory controller 403 and/or the memory 3501 are not, however, one of the *first blocks* identified by the Examiner (i.e., system bus bridge 402 and bus masters 1-4). The "Memory Bus," therefore, does not couple one of the first blocks to one of the second blocks external to the chip as recited in claims 1, 5, and 34. Date, Fig. 4. Since Date does not disclose an external bus that couples one of the first blocks on the chip to one of the second blocks external to the chip, Date does not anticipate claim 1.

Claim 1 further recites *a single on-chip multi-jurisdictional arbiter adapted to receive requests for ownership of the system bus and of the external bus, ... to transmit a first grant signal to the dual first block regarding a first ownership of the external bus...* Date shows a single bus arbiter labeled G Bus arbiter 406 that is connected to the system bus 404. Date, Fig. 4. The function of the G Bus arbiter as it relates to specific grant of ownership of the external bus, however, is not enabled by Date. The G Bus arbiter gains ownership of the external bus similarly to the prior art in Fig. 2A disclosed in the present application, where the external bus is a slave to the system bus master. Figure 2A; Specification page 3, lines 27-31 and page 4, lines 1-2; Date, column 29, lines 60-65 and column 30, lines19-26, where Date illustrates how the G Bus arbiter 406 allows bus master 1 to retrieve data from system memory using both the G Bus 404 and the "Memory Bus" by only granting bus privilege to the G Bus 404. Since Date's bus ownership scheme is similar to that of prior art disclosed in Fig. 2A, the G Bus arbiter does not receive requests for ownership of the external bus or transmit a first grant signal to the dual first blocks regarding first ownership of the external bus as recited. Date, therefore, does not anticipate claim 1.

Claim 5 recites *an external bus ... and a plurality of first blocks on the chip coupled directly with the system bus, wherein at least one of the first blocks is an external memory controller coupled to the external bus and adapted to control at least one memory device that is external to the chip ...* Date's external bus, as we argue above regarding claim 1, appears to be the bus labeled "Memory Bus" coupled between the memory controller 403 and the system memory 3501, and not the IO Bus 405 as the Examiner alleges. Date, Fig. 4 and Fig 35. Since the memory controller 403 is not one of the first blocks then Date does not anticipate claim 5. Fig. 4.

Claim 5 further recites *a plurality of first blocks on the chip coupled directly with the system bus, wherein ... one of the first blocks is a multi-jurisdictional multi-channel general direct memory access block that is coupled with the external memory controller...* Date shows the system bus 404 coupled to the system bus bridge 402 and bus masters 1-4. Date, Fig. 35. Date does not show a multi-jurisdictional multi-channel general direct memory access block that is one of these first blocks. Date, Fig. 4 and Fig. 35. Since the multi-jurisdictional multi-channel general direct memory access block is not one of the first blocks connected directly to the system bus 404, Date does not anticipate claim 5. Date, Fig. 4.

Claim 9 is dependent from claim 5 and is, therefore, not anticipated by Date. For completeness, however, we note claim 9 further recites *an on-chip multi-jurisdictional arbiter to transmit a first grant signal to one of the first blocks regarding a first ownership of the system bus and to transmit a second grant signal to the external memory device regarding a second ownership of the external bus that is concurrent with the first ownership.*

Date does not enable the transmitting of a second grant signal regarding second ownership of the external bus concurrent with the first ownership of the system bus since the G Bus arbiter does not grant privilege directly to a bus master concerning ownership of only the external bus. See, claim 1 argument concerning Date's bus ownership scheme as it relates to the prior art disclosed in Figure, 2A and Specification, page 3, lines 27-31 and page 4, lines 1-2 of the present application. Date, therefore, does not anticipate claim 9.

Claim 18 recites

determining whether at least one of the system bus and the external bus would be idle if the first request were granted; and

if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request.

Claims 23 and 31 recite similar limitations. Date does not enable the execution of instructions that determine if either the system bus or the external bus would be idle if a first request for ownership of one of the two buses were granted. See, the claim 1 argument concerning Date's bus ownership scheme as it relates to the prior art disclosed in Figure 2A and Specification, page 3, lines 27-31 and page 4, lines 1-2 of the present application. Date shows a G Bus arbiter 406 that can only grant a request for ownership of the single system bus that, in turn, has the optional ownership of the slave external bus, but it does not disclose the G Bus arbiter 406 determining whether the external bus is idle during the given cycle when permission for the system bus is granted. Date, Fig. 4 and Fig. 35, column 30, lines 19-26. Date, moreover, does not enable the selecting, or granting, of a second request for the use of the idle external bus concurrent with the first request for the use of the G Bus 404 because it does not enable the determining whether that the system bus or external bus is idle if the first request is received. Since Date does not enable the determining of when a bus is idle, if a first request were granted, it cannot select or grant a second request for ownership of that idle bus concurrently with a first grant of ownership. Date, therefore, does not anticipate claim 18, nor is it obvious to a person of ordinary skill in the art.

Claim 21 recites

granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system; and

then granting a request by the mJmCGDMA block to control only an external bus in an off-chip system.

Date does not disclose an on-chip mJmCGDMA block in either its drawings or its specifications, nor does the Examiner contend that one is present. Date, therefore, does not anticipate claim 21, nor is it obvious to a person of ordinary skill in the art.

Claim 23 recites

identifying the buses that would be idle if the first request were performed;

selecting a second one of the requests that can be performed by at least one of the system bus and the external bus that would be idle if the first request were performed; and

granting the second request concurrently with granting the first request.

As we argue above regarding claim 18, Date does not enable the identifying of an idle external bus if a request for the G Bus 404 were performed. Date, Fig. 4. It merely grants a request to the G Bus master to use of the G Bus 404, which further allows the G Bus master the optional use of the slave external bus. See, the claim 1 argument concerning Date's bus ownership scheme as it relates to the prior art disclosed in Figure 2A and Specification, page

3, lines 27-31 and page 4, lines 1-2 of the present application. Moreover, as we argue above regarding claim18, Date does not enable the selecting, or granting, of a second request for the use of the idle external bus concurrent with the first request for the use of the G Bus 404 because it does not enable the identification that the external bus is idle. Date, therefore, does not anticipate claim 23.

Claim 28 recites *having an on-chip CPU block, an on-chip functional block, at least one on-chip system bus for connecting the on-chip blocks* ... The Examiner identifies the on-chip CPU block as item 401, the other on-chip functional block is the system bus bridge 402 and the system bus is the G Bus 404. Date, Fig. 4 and Fig. 35. The G Bus 404, however, is not connected to the CPU block 401 and therefore the system bus cannot connect the CPU block 401 to the system bus bridge 402. Date, Fig. 4 and Fig. 35. Since the recited on-chip blocks are not connected via the system bus, Date does not anticipate claim 28.

Claim 28 further recites

... an on-chip DRAM refresh controller...

receiving a plurality of requests, a first one of which being from the DRAM refresh controller...

examining whether a second one of the remaining requests is for using only the system bus; and

if so, granting the first and second requests to be performed concurrently.

The Examiner alleges Date shows a DRAM refresh controller, labeled memory controller 403, and a system bus, labeled G Bus 404. Date, Fig. 4 and Fig. 35. In Date, the requests for system bus ownership appear that they must be received by the G Bus arbiter 406. Date, column 9, lines 27-29; column 30, lines 14-42; Fig. 4 and Fig 35. Date does not enable the G Bus arbiter 406 to receive a request from the DRAM refresh controller 403. Date enables the DRAM refresh controller 403 to self-refresh within its internal cache memory 702. Date, column 13, lines 29-39, Fig. 4, and Fig. 7. Further, Date does not enable the examining whether a second one of the requests is for using only the system bus. See the claim 1 argument concerning Date's bus ownership scheme as it relates to the prior art disclosed in Figure 2A and Specification page 3, lines 27-31 and page 4, lines 1-2 of the present application. Date shows the G Bus arbiter 406 granting ownership to the system bus, but does not disclose if the system bus master uses the slave external bus during the given cycle. Date, column 30 lines 14-51, demonstrating three separate grants of system bus privilege, by the G Bus arbiter, are consecutively performed, but failing to examine when the system bus is only in use. Date, therefore, does not anticipate claim 28.

Claim 31 recites

determining whether at least one of the system bus and the external bus would be idle if the first request were granted; and

if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request.

As we argued above regarding claim 18, Date does not enable a method for determining whether the system bus or the external bus would be idle if the first request of ownership of either bus were granted. See, the claim 18 argument concerning the identification of an idle bus if the first request were granted. Also as we argued above regarding claim 18, Date does not enable the selecting or granting of a second request for the use of only the idle bus that is concurrent with the first request. See, the claim 18 argument concerning the selecting and granting of a second request for the use of an idle bus. Date, therefore, does not anticipate claim 31.

Claim 34 recites *having an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block, an on-chip functional block, at least one on-chip system bus for connecting the on-chip blocks, and an external bus for the mJmCGDMA block to exchange data with an off-chip device...* As we argue above regarding claim 21, Date does not disclose an on-chip mJmCGDMA block in either its drawings or its specifications, nor does the Examiner contend that one is present. Date, therefore, does not anticipate claim 34.

Independent claims 1, 5, 18, 21, 23, 28, 31 and 34 are useful, novel, and not obvious over Date and all other cited prior art. Dependent claims 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 19, 20, 22, 24, 25, 26, 27, 29, 30, 32, 33 and 35 are likewise useful novel, and not obvious over Date and all other cited prior art. Claims 1-35 are, therefore, in condition for allowance.

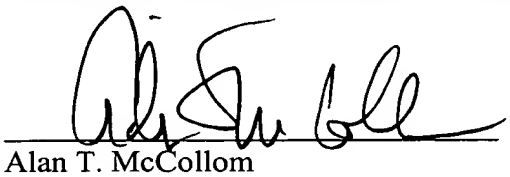
CONCLUSION

Applicants request reconsideration and allowance of claims of all claims as amended. Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613